



**Barcelona
Supercomputing
Center**
Centro Nacional de Supercomputación



**28th Ada-Europe
International Conference on
Reliable Software Technologies
(AEiC 2024)
11-14 June 2024, Barcelona, Spain**

FINAL PROGRAM

<http://www.ada-europe.org/conference2024>

In cooperation with



PRESENTATION

The 28th Ada-Europe International Conference on Reliable Software Technologies (AEiC 2024) returns to Spain, for the first time in Barcelona, from the 11th to the 14th of June.

The conference is the latest in a series of annual international conferences started in the early 80's, under the auspices of Ada-Europe, the international organization that promotes knowledge and use of Ada and Reliable Software in general, into academic education and research, and industrial practice.

The conference is an established international forum for providers, practitioners and researchers in reliable software technologies. The conference presentations will illustrate current work in the theory and practice of developing, running and maintaining challenging long-lived, high-quality software systems for a variety of application domains including manufacturing, robotics, avionics, space, transportation.

The conference program includes two core days with special sessions featuring presentations of invited experts, peer-reviewed academic papers, industrial presentations, and work-in-progress talks and posters. The conference program is bracketed by one day of tutorials and hackathon, and one day with four satellite events: the 9th DeCPS workshop on “Challenges and new Approaches for Dependable and Cyber-Physical Systems

Engineering”, the “3rd ADEPT: AADL by its practitioners” workshop, the “Safe AI” workshop, and the “Ada Developers Workshop”.

The event also includes social events: a welcome event on Tuesday, at the end of the afternoon tutorials, with a visit to the Barcelona Supercomputing Center, and a cocktail dinner in a nearby restaurant; a banquet on Wednesday, at the emblematic restaurant "7 portes" by the seaside, to savour the finest flavours of the Catalan and Mediterranean cuisines, and a chill-out event at the Moritz Barcelona Brewery, the brewery of the first beer of Barcelona, on Thursday after the core conference closure.

Barcelona is a city renowned for its vibrant culture and rich history. With its world-class research institutions and cutting-edge facilities, like the Barcelona Supercomputing Center (BSC), the ALBA Synchrotron light facility, the Barcelona Biomedical Research Park (PRBB), or the Barcelona Science Park (PCB), Barcelona embodies innovation and excellence in the scientific realm. From the iconic architecture of Antoni Gaudí to the bustling streets of the Gothic Quarter, delegates attending AEiC 2024 can immerse themselves in a blend of tradition and modernity. Moreover, the city's renowned culinary scene and vibrant nightlife provide opportunities for networking and cultural exploration!

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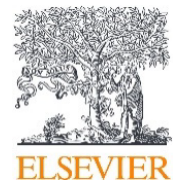
OVERVIEW OF THE CONFERENCE PROGRAM

	Morning	Before Lunch	After Lunch	Afternoon	Evening		
Tuesday, June 11th <i>Tutorials and Hackathon</i>	Tutorial 1: <i>Lock-free programming in Ada 2022</i>		Tutorial 2: <i>Ada for business applications</i>		Welcome Visit and Dinner		
	Tutorial 3: <i>Rust Fundamentals</i>		Tutorial 4: <i>Concurrency and Parallelism in Rust</i>				
	Tutorial 5: <i>Modeling concurrent state machines in TLA+</i>		Tutorial 6: <i>Introduction to the development of safety critical software</i>				
	Tutorial 7: <i>METASAT: programming high-performance RISC-V technologies for space</i>		Tutorial 8: <i>Introduction to certifiable general purpose GPU programming for safety-critical systems</i>				
	Hackathon: <i>Optimizing AI-driven workflows within a mission-critical cyber-physical system</i>						
Wednesday, June 12th <i>Technical Presentations</i>	Keynote Talk	Session 1: <i>Fault Tolerance and Reliability in Heterogeneous Systems</i>	Invited Talk	Session 2: <i>Software Verification and Code Generation</i>	Invited Talk	Session 3: <i>Security and Safety in Embedded Systems</i>	Conference Banquet
Thursday, June 13th <i>Technical Presentations</i>	Panel	Session 4: <i>Machine Learning and Optimization for Embedded Systems</i>	Session 5: <i>Real-Time Systems and Their Analysis</i>		Session 6: <i>Advancements in RTOS and Embedded Software Development</i>	Chill-out event	
Friday, June 14th <i>Workshops</i>	<i>Workshop on Challenges and New Approaches for Dependable and Cyber-Physical System Engineering (DeCPS 2024)</i>						
	<i>AADL by its practitioners Workshop (ADEPT)</i>						
	<i>Safe AI: Enabling the use of AI in Safety-Critical Systems</i>						
	<i>Ada Developers Workshop</i>						

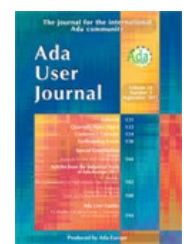
PROCEEDINGS

The papers presented at the conference are channelled into distinct proceedings.

The journal-track papers that will successfully complete their cycle of peer-review and revisions, will appear in a dedicated, Special Issue of Elsevier's **Journal of Systems Architecture**. In order to speed the publication cycle, the papers assigned to that Special Issue will appear asynchronously, as soon as ready individually. Their individual availability in Open Access for everyone will be announced on the Ada-Europe website dedicated to AEiC 2024. Expectedly, such papers will begin to appear as of September 2024.



The papers presented in the industrial track, the work-in-progress track, and the collocated workshops, DeCPS and ADEPT, will all appear in subsequent issues of the **Ada User Journal**, expectedly from June 2024 right after the end of the conference.



CONFERENCE VENUE

The conference will take place in two near locations of the UPC Campus Nord. Tutorials (Tuesday) and Workshops (Friday) will be hosted in the BSC-Repsol Building, while the main conference (Wednesday and Thursday) will be hosted in the Vèrtex UPC Building.



The BSC-Repsol Building, functioning since 2021, is a new 12.000m² facility housing more than 500 workers and the recently inaugurated MareNostrum 5 supercomputer. The building has 4 office floors, more than 30 meeting rooms and training rooms, and auditorium and various meeting points.



The BSC-Repsol building is connected, through a walkway, to what has been the center's most emblematic building, the Torre Girona chapel, which until recently housed the MareNostrum 4. In the future, the chapel will host two quantum computers and other experimental architectures.

The Vertex building, also on the North Campus of the Polytechnic University of Catalonia (UPC), offers a series of classrooms where both training for the UPC's administrative and service staff and other courses and congresses that require space for parallel sessions are held. For AEiC2024, we will be using the "Sala d'Actes" (or Conference Hall), with a capacity for 160 people.



Participants registration will be open Tuesday before tutorials (8:30 - 9:00) and during the welcome event (17:45 - 19:00) at BSC main entrance; before conference starts on Wednesday (8:30 - 9:00) and Thursday (9:00 - 9:15) at UPC-Vertex building floor -1; and Friday before workshops (8:45 - 9:00) at BSC main entrance.

INVITED SPEAKERS

Wednesday, June 12th, morning

Keynote Talk

Strategies to build safety relevant high-performance HW/SW platforms for critical embedded systems

FRANCISCO J. CAZORLA & JAUME ABELLA
BARCELONA SUPERCOMPUTING CENTER, SPAIN

Abstract

The increasing autonomy requirements of critical embedded systems (CES) in a variety of domains, including automotive, space, avionics, and robotics, rely on AI software. The high-performance requirements of AI software call for the adoption of MPSoCs capable of providing the required performance levels. However, this trend towards more complex hardware and software in CES poses significant challenges on functional safety. Challenges relate to non-obvious interactions across applications and tasks, with arbitrarily large impact on performance and also functional correctness. This calls for hardware and software solutions that mitigate these risks.

In this talk we will delve into two sets of technologies to mitigate the risks associated to the increasing complexity of the platforms needed for future CES, namely (1) software-only solutions based on advanced platform testing and configuration, and (2) hardware modules providing observability, controllability, and support for safety measures.

In terms of software-only solutions, we will present methods and technologies to identify key performance features relevant for multicore interference in high-performance MPSoCs, and to configure QoS knobs to mitigate interference while preserving performance, as well as software technologies to generate stressful scenarios relevant for Worst-Case Execution Time (WCET), and to enable WCET estimation in the context of multi-provider software with IP restrictions.

In terms of hardware solutions, we will present our strategy to extend high-performance MPSoCs with features to enable their use in safety-relevant scenarios without impacting meaningfully performance. In particular, we will present several modules for advanced multicore observability and quota control (SafeSU), flexible performance testing (SafeTI), multiple flavors of

diverse redundancy (SafeDM, SafeDE, SafeLS), and platform monitoring and reconfiguration (SafeTCO).

Short Bio



Dr. Francisco J Cazorla, co-leads the CAOS research group at BSC. His area of research includes the safe use of aggressive processor designs (e.g. multicore designs) in critical embedded systems. Dr. Cazorla has led 3 European Projects (PROARTIS, PROXIMA, and MASTECS) and has been ERC Consolidator Grantee (SuPerCom) on this topic. He has also led several projects funded by the European Space Agency (ESA). He was the confounder of Maspatechnologies, a BSC spin-off specialized in software verification technologies of the temporal behavior of multicore processors.



Dr. Jaume Abella, co-leads the CAOS research group (embedded systems group) at BSC. Dr. Abella leads the HE SAFEXPLAIN project, and is (has been) the PI at BSC of another 10 EU projects on enabling the use of high-performance hardware and software, as well as AI in safety-critical systems. Jaume co-leads the OpenHW Group Safety&Security Task Group and RISC-V International SIG-Safety. Dr. Abella holds 15 patents issued, has published around 250 papers in peer-reviewed conferences and journals, has co-advised 15 PhDs and 20 Master theses, and co-founded a successful spinoff providing software services in avionics and automotive.

Thursday, June 13th, morning

Panel

AI for Safety-Critical Systems: How "I" Should the AI be?

Short Bio of Invited Experts

CRISTINA SECELEANU (MODERATOR)
MÄLARDALEN UNIVERSITY, SWEDEN



Prof. Dr. Cristina Seceleanu is Professor of Computer Science and Docent at MDU, Networked and Embedded Systems (NES) division, and research leader of the Computer and Data Science (CDS) research direction. She received a MSc. in

Electronics from Polytechnic University of Bucharest, Romania, in 1993, and a Ph.D. in Computer Science from Åbo Akademi and Turku Centre for Computer Science, Åbo/Turku, Finland, in Dec. 2005. Her research focuses on developing formal models and verification techniques for designing predictable real-time, adaptive and autonomous systems.

KERSTIN BACH

NORWEGIAN UNIVERSITY OF SCIENCE AND TECHNOLOGY, NORWAY



Prof. Dr. Kerstin Bach is a professor of Artificial Intelligence at the Norwegian University of Science and Technology (NTNU) and holds the role of Research Director at the Norwegian Research Center for AI Innovation (NorwAI). She

commenced holds a PhD from the university of Hildesheim and worked as a researcher at the German Research Center for AI (DFKI), where she developed decision support systems for various industries. Throughout her career, Kerstin has undertaken significant responsibilities, notably as the driving force behind myCBR, an open-source tool adopted in research and industry projects across Europe. Following the completion of her Ph.D., Kerstin joined Verdande Technology, a Trondheim-based AI startup, where she held roles as both a research scientist and software engineer before eventually joining the faculty at NTNU.

IRUNE YARZA

IKERLAN, SPAIN



Dr. Irune Yarza is an Industrial Electronic and Automation Engineer by the University of Deusto, master's in advanced electronic systems by the ETSI in Bilbao (2016), and Ph.D. in Computer Science by the

University of Oldenburg (2019). She joined IKERLAN as a researcher in 2015, becoming part of the Real-Time Systems team in the Reliable Embedded Systems area. She obtained her Ph.D. in Computer Science at the University of Oldenburg (Germany), completing stays at OFFIS - Institute for Information Technology. Subsequently, she has been part of the Cybersecurity and Safety Systems area within the Cybersecurity and Safety Methodologies team. With her participation in European projects, her main research activity today focuses on functional safety. Additionally, she has participated in

various R&D projects in the field of real-time safety-critical embedded systems, mainly in the lift and automotive sectors. She holds the Functional Safety Engineer certification from TÜV Rheinland according to the ISO-26262 and IEC-61508 standards.

MARTA BARROSO

BARCELONA SUPERCOMPUTING CENTER, SPAIN



MSc. Marta Barroso Isidoro began her academic journey with a Bachelor's in Computer Science at UPC, followed by a Master's in AI, focusing her thesis on utilizing biosensors in psychiatric hospitals to

monitor patient movement, particularly when they leave their beds. Her current role at the Barcelona Supercomputing Center involves working with the HPAI research group, where she applies her expertise in Machine Learning and Deep Learning to projects like ciberes-uci-covid and KnowlEdge, generating valuable insights for healthcare. Marta's problem-solving style emphasizes attention to detail and innovation, using advanced computational methods to tackle healthcare challenges. She's also pursuing research in large language models to contribute to this field.

Wednesday, June 12th, afternoon

Invited Talk

Simplifying the life-cycle management of complex application workflows

ROSA MARIA BADIA

BARCELONA SUPERCOMPUTING CENTER, SPAIN

Abstract

With Exaflop systems already here, high-performance computing (HPC) involves larger and more complex supercomputers. At the same time, the user community is aware of the underlying performance and eager to leverage it by providing more complex application workflows to leverage them. Moreover, current application trends aim to use data analytics and artificial intelligence combined with HPC modelling and simulation. However, the programming models and tools are different in these fields, and there is a need for methodologies that enable the development of workflows that combine HPC software, data analytics, and artificial intelligence.

PyCOMPSs is a parallel task-based programming in Python. Based on simple annotations, it can execute sequential Python programs in parallel in HPC clusters

and other distributed infrastructures. PyCOMPSs has been extended to support tasks that invoke HPC applications and to combine them with Artificial Intelligence and Data analytics frameworks. PyCOMPSs also supports fault-tolerance at the task level, giving flexibility to cancel part of the workflow due to faults. It also implements a checkpointing and restart feature to support major failures. In addition, to help with the overall workflow lifecycle management, we have defined the HPC Workflows as a Service (HPCWaaS) methodology that aims to provide tools to simplify the development, deployment, execution, and reuse of workflows. In particular, we will describe the Container Image Creation service, which automates the creation of container images tailored to a specific HPC platform.

Short Bio



Dr. Rosa M. Badia holds a PhD on Computer Science (1994) from the Technical University of Catalonia (UPC). She is the manager of the Workflows and Distributed Computing research group at the

Barcelona Supercomputing Center (BSC). She is considered one of the key researchers in Parallel programming models for multicore and distributed computing due to her contribution to task-based programming models during the last 15 years. The research group focuses on PyCOMPSs/COMPSs, a parallel task-based programming distributed computing, and its application to the development of large heterogeneous workflows that combine HPC, Big Data, and Machine Learning. The group is also doing research around the dislib, a parallel machine learning library parallelized with PyCOMPSs. Dr. Badia has published near 200 papers in international conferences and journals on the topics of her research. She has been very active in projects funded by the European Commission in contracts with industry, and she has been the PI of the EuroHPC project eFlows4HPC. She is a member of HiPEAC Network of Excellence. She received the Euro-Par Achievement Award 2019 for her contributions to parallel processing, the DonaTIC award, category Academia/Researcher in 2019 and the HPDC Achievement Award 2021 for her innovations in parallel task-based programming models, workflow applications and systems, and leadership in the high performance computing research community. In 2023, she has been invited to be a member of the Institut d'Estudis Catalans (Catalan academy).

Wednesday, June 12th, afternoon

Invited Talk

The Compute Continuum: An Efficient Use of Edge-to-Cloud Computing Resources

EDUARDO QUIÑONES

BARCELONA SUPERCOMPUTING CENTER, SPAIN

Abstract

There is the need for gluing edge, cloud and HPC technologies into a unified compute continuum solution to manage and analyse the complete lifecycle of data, and on top of it, provide new frameworks to enable users to easily describe complex data analytics workflows to be deployed on the compute continuum. Towards this direction, this presentation will identify the three main key challenges that are needed to be addressed: (1) optimize current data infrastructures and AI & Big-data frameworks to jointly address data processes and analytics methods; (2) develop orchestration techniques to select the most appropriate set of computing resources; and (3) increase the interoperability between the most common programming practices and execution models used across the compute continuum, i.e., HPC, edge and cloud computing resources, to effectively address the diverse characteristics of data.

Short Bio



Dr. Eduardo Quiñones is a senior researcher in the Department of Computer Science at the Barcelona Supercomputing Center (BSC). He received his Ph.D. in computer science from the Universitat Politècnica de Catalunya (UPC) in Barcelona in 2008.

His research interests are strongly tied to next generation industry requirements for critical real-time systems spanning future processor architecture, operating system and compiler designs. Eduardo has experience in international research projects, including European Projects and European Space Agency (ESA) projects. He collaborates with key multinational companies in the avionics, automotive and space domains, including Airbus Defense and Space, Denso, Infineon, Kalray, Thales and Honeywell, and with the main European research institutions.

TUTORIALS: TUESDAY, JUNE 11TH

Morning, half day

T1: Lock-Free Programming in Ada-2022: Implementing a work-stealing scheduler for Ada-2022's light-weight parallelism

S. Tucker Taft, AdaCore

Abstract

This tutorial will introduce the attendee to the use of the new packages in the System.Atomic_Operations subsystem for lock-free programming in Ada, as well as the concept of a work-stealing scheduler for light-weight threads. We will review the implementation of an efficient double-ended queue (deque) for a work-stealing scheduler using the features of the Atomic_Operations subsystem, and investigate some of the tradeoffs when using lock-free data structures. Finally, we will experiment with the work-stealing scheduler, to understand some of the subtleties of Ada 2022's light-weight parallelism features and how best to use work-stealing to support them.

Level: *Intermediate to Advanced programming in Ada.*

Reasons for attending

- Gain exposure to lock-free primitives and how they can be used to implement efficient lock-free data structures.
- Build an understanding of the scheduling challenges for light-weight threads, and some of the practicalities of creating efficient parallel programs.

Presenter

S. Tucker Taft has been the Director of Language Research at AdaCore since 2011. Prior to that Tucker was founder and lead engineer at SofCheck for nine years, and a language designer and compiler engineer for 22 years at Intermetrics and its follow-ons. Tucker was the technical lead for the project that developed Ada 95, and has been a member of the Ada Rapporteur Group which developed Ada 2005, Ada 2012, and Ada 2022. Tucker is also the designer and implementor of the ParaSail parallel programming language.

Afternoon, half day

T2: Ada for Business Applications

Gautier de Montmollin, Ada Switzerland

Abstract

The Ada language was originally developed as a one-fits-all language designed to simplify the language landscape of the US Department of Defense. One particularly highlighted application area was safety-critical, embedded applications, where the Ada language actually excels due, notably, to its strong typing and range checks. However, the "one-fits-all" aspect was quickly and unfortunately lost on the roadside, although it is real. Two successful ingredients of the language in a broad variety of applications are very simple: modularity and superior error detection, which help developing applications of any size – and importantly, applications that do their job correctly. However, a third key ingredient – free or cheap, and easily available programming components – is only now, decades later, materializing thanks to the Alire crate system. We show in this tutorial, with concrete examples, how Ada is a better tool in rapid development of very different kinds of software like user interfaces, number crunching (scientific applications), simulations, data acquisition, and mixes of all that.

Level: *No prerequisite needed.*

Reasons for attending

- Discover experiences with Ada outside the Military-Space-Avionics-Railways "ghetto"
- Brainstorm, experiment, discuss what is good and what is missing in the Ada ecosystem

Presenter

Gautier de Montmollin is a software developer. He holds a PhD in mathematics from the University of Neuchâtel, Switzerland. His quest for both run time and development time efficiency has trapped him with the Ada language which he has the luck to use professionally (formerly in finance, now in robotics) and for private projects as well. He has presented professional and private projects at various Ada-Europe and FOSDEM conferences.

Morning, half day

T3: Rust Fundamentals

Luis Miguel Pinho and Tiago Carvalho, ISEP, Portugal

Abstract

This tutorial will provide attendees with the basics of programming in the small in Rust, covering data types, control-flow constructs, statements, expressions and functions, as well as some aspects of object-oriented programming and generics. The tutorial will then focus on the (somehow) complex mechanisms of Rust for mutability and ownership of variables, showing how Rust tracks the lifetime and scope of all references in a program during compilation, enforcing memory safety and preventing concurrent data races, providing flexibility without requiring the use of a garbage collector. The tutorial will also present two of the most relevant concepts used for functional style of programming in Rust: closures and iterators, showing how these concepts can be used together to implement programs in a declarative style.

Level: *Intermediate.*

Attendees should be familiar with programming languages in general.

Reasons for attending

- Understand the main concepts behind the Rust programming language
- Learn how Rust addresses memory safety and programming in the small
- Learn the most relevant concepts used for functional style of programming in Rust

Presenters



Luis Miguel Pinho is a Professor at the Department of Computer Engineering - School of Engineering of the Polytechnic Institute of Porto, and Senior Researcher at the INESC TEC Associated Laboratory. He promotes and leads activities in, among others, real-time parallel programming models, reliable software, and edge computing. He has published more than 150 papers in international conferences and journals in the area of real-time embedded systems, and has been general/program chair of several international conferences. He is a member of ISO/IEC JTC1/SC22/WG9, and senior member of ACM and IEEE. He was Editor-in-Chief of the Ada User Journal, and is currently Technical Editor of ACM SIGAda Ada Letters.



Tiago Carvalho is a researcher and invited professor at the School of Engineering of the Polytechnic Institute of Porto, where he works in activities related to real-time parallel programming and timing analysis. He has a PhD in Compilers and a MSc degree in Computer Engineering from the Faculty of Engineering of the University of Porto (FEUP), where he is an invited assistant professor. Tiago has experience in compiler-related topics such as domain-specific languages and compiler optimizations.

Afternoon, half day

T4: Concurrency and Parallelism in Rust

Luis Miguel Pinho and Tiago Carvalho, ISEP, Portugal

Abstract

This tutorial will provide attendees with some of the available mechanisms and libraries of Rust to program concurrent and parallel applications. The tutorial will start with the basic concurrency mechanisms provided in the Rust language and its standard library: threads, channels, shared data support with the Atomically Reference Counted type, and thread synchronization. The Rust language provides by itself a limited set of mechanisms for concurrency, giving preference to the implementation of more advanced mechanisms through libraries. Therefore, the tutorial will briefly present some of the common libraries for concurrency (such as `parking_lot` or `crossbeam`), focusing afterwards in more advanced libraries for concurrent and parallel applications: the `ThreadPool` library, which provides a simple thread pool approach to execute lightweight tasks and `Rayon`, a data-parallelism library that makes it easy to convert sequential computations into parallel by using iterators.

Level: *Advanced.*

Attendees should be familiar with the Rust programming language (possibly by attending the morning tutorial).

Reasons for attending

- Learn the main features provided by the Rust language to support safe concurrency
- Learn some of the main libraries available for concurrent and parallel programming in Rust

Presenters

See presenters of Tutorial 3

Morning, half day**T5: Modeling Concurrent State Machines in TLA+**

J. Germán Rivera, Tesla

Abstract

Concurrent (communicating) state machines are present in many embedded software systems. Interactions between these state machines cannot be easily described in graphical form at a level of detail precise enough to check their correctness in all possible cases. State transitions in one state machine may affect transitions in another state machine and unintended races can be very hard to detect in testing and can easily escape to production. TLA+ is a discrete-math-based modeling language for specifying concurrent state machines. Its companion model checking tool (TLC) can help catch bugs in the state machine design. With model checking, all possible state transitions and races between concurrent state machines can be simulated to find concurrency bugs. This tutorial introduces the basics of TLA+ and how to use it to model concurrent state machines and to check them with TLC, to verify if they satisfy their intended correctness properties.

Level: *Introductory (Basic knowledge of discrete mathematics can be helpful)*

Reasons for attending

Learning TLA+ on your own may be intimidating at first, but after attending this tutorial, attendees will be able to explore the TLA+ resources available online, with more confidence, learn from more complex TLA+ modeling examples and start creating their own models.

Presenter

J. Germán Rivera is a senior staff software engineer at Tesla, where he develops low-level embedded software for automotive system-on-chip platforms. He has 34 years of industry experience developing system-level software. He has also held software development positions at Google, NXP, Microsoft, Cisco, IBM, NetApp and HP. He holds a Master of Software Engineering degree from Carnegie Mellon University (USA) and a Bachelor's degree in Computer Science, from the University of Los Andes (Colombia). In his spare time, he writes Ada/SPARK embedded software for hobby projects, in which he also experiments with practical applications of formal methods.

Afternoon, half day**T6: Introduction to the Development of Safety Critical Software**

Jean-Pierre Rosen, Adalog, France

Abstract

This tutorial presents the fundamental notions that make the development of safety critical software different from the development of more casual software. It presents the context, the applicable standards, and the techniques used for achieving high reliability. It explains why Ada and Spark are especially suited for writing safety critical software. Although required for demanding applications, the general principles that can be applied to, and help improve, all kinds of software development.

Level: *Intermediate.*

Expected audience experience: Casual knowledge of Ada.

Reasons for attending

- Understand the stakes of the development of safety critical software
- Learn the various rules governing the development of safe software, and understand their motivation
- Consider the tools that are available to improve quality and safety of software
- Apply some principles to more casual software for higher reliability

Presenter

JP Rosen is a professional teacher, teaching Ada (since 1979, it was preliminary Ada!), methods, and software engineering. He runs Adalog, a company specialized in providing training, consultancy, and services in all areas connected to the Ada language and software engineering. He is chairman of Ada-France.

Adalog offers regularly on-site and off-site training sessions in Ada. Adalog is regularly performing reviews and safety assessments for safety critical software, especially in the domain of railway system.

Morning, half day**T7: METASAT: Programming High Performance RISC-V Technologies for Space**

Leonidas Kosmidis, Barcelona Supercomputing Center (BSC), Alejandro Calderon, Ikerlan, Aridane Alvarez

Suarez, fentISS, Lorenzo Lazzara, Collins Aerospace, Eckart Göhler, OHB

Abstract

METASAT is a Horizon Europe project which develops a holistic and modular model-based framework to design and test software modules that target open architecture hardware, high-performance computing platforms for the space and aviation domain. It particularly focuses on open standards and open source technologies such as the RISC-V open ISA, open parallel programming standards like OpenMP, OpenCL and OpenGL SC and AADL. In terms of hardware, METASAT is currently developing a RISC-V based multicore platform using the Frontgrade Gaisler's NOEL-V processor, integrated with the SPARROW short vector AI accelerator and the RISC-V Vortex GPU. On the model-based design toolchain, it relies on ESA's TASTE open source toolchain, which is extended with capabilities targeting the complexity of high performance platforms for space. Almost all project developments will be available as open source at the end of the project (December 2024). This tutorial aims to provide an introduction and a hands on approach of the project developments

Level: *Introductory*

Afternoon, half day

T8: Introduction to Certifiable General Purpose GPU Programming for Safety-Critical Systems

Leonidas Kosmidis, Barcelona Supercomputing Center (BSC), Rod Burns, Codeplay/Intel, Verena Beckham, Codeplay/Intel

Abstract

GPUs are currently considered from all safety critical industries (automotive, avionics, aerospace, healthcare etc) to accelerate general-purpose computations and meet performance requirements, which are not possible with the legacy, single-core processors used in these domains. However, most of the R&D in companies from these domains is focused on proof of concepts, which demonstrate the capabilities of employing GPUs in these domains, ignoring the certification challenges introduced by GPUs. In this tutorial, we will teach the attendees how general purpose GPU code can be developed and certified according to safety critical standards used in these industries, using open standards such as Khronos APIs as well as AdaCore's experimental compiler for programming NVIDIA GPUs using Ada/SPARK. This is a very timely topic since it also introduces the latest GPU programming API for safety critical systems, SYCL SC, which is under development by Khronos, in a working group created in March 2023, in which the organisers are actively involved. Leonidas Kosmidis serves as the Working Group Outreach Officer while Verena Beckam is the Working Group Chair. In addition, both organisers are contributing to these open standard technologies in Horizon Europe projects, METASAT (<https://metasat-project.eu/>) and SYCLOPS (<https://www.syclops.org/>).

Level: *Introductory.*

The tutorial attendees must be familiar with C++ and Ada/SPARK. Moreover, understanding of safety critical systems and familiarity with at least one safety standard (ISO 26262, DO-178C, ECSS) and safety critical code development guidelines (i.e. MISRA C/C++) is desirable but not required.

HACKATHON: TUESDAY, JUNE 11TH

Full day

Hackathon: Optimizing AI-driven workflows within a mission-critical cyber-physical system

Damien Gratadour (CNRS – Observatoire de Paris), Bartomeu Pou Mulet (Barcelona Supercomputing Center)

Abstract

The largest ground-based telescopes will soon reach ~40m diameter and provide the angular resolution and

collecting area to perform the required measurements to detect fainter exoplanets. But to reach the required contrast, they must overcome optical distortion induced by atmospheric turbulence. In order to compensate for such distortion and eventually maximize achievable contrast, Adaptive Optics (AO) technologies were developed for astronomy starting in the 1990s, and is now essential for the current largest optical telescopes. In an AO system, a wavefront sensor (WFS) is used to measure the atmospheric distortion at a high frame rate, which is then compensated with a deformable mirror (DM). The sub-system linking those

two components, responsible for interpreting wavefront measurements into actual commands to actuators for the DM, is the real-time controller (RTC). This sub-system, that can be seen as a mission-critical cyber-physical system, must operate at high speed (~ kHz rate) to catch up with rapidly changing optical turbulence of the atmosphere. Indeed, it requires to ingest raw data streaming from sensors, to be processed through batched-centroiding and matrix-vector multiplies, to provide several millions of commands per second to the deformable optics.

Our team has proposed to use current deep learning techniques to pre-process WFS images for denoising purposes. For that, an architecture similar to the denoising autoencoder is used, which learns a map from noisy input to noise-free output. The proposed architecture consists of convolutional layers together with maxpool operations (current state-of-the-art in image processing tasks). While the initial work on the denoising autoencoder and convolutional autoencoder consisted on learning more robust representations in the hidden layers and use those as a initialisation point for other networks in tasks such as image classification, it can be applied for denoising purposes.

In this hackathon, we propose to enhance this denoising module, as part of a comprehensive AO RTC pipeline.

This hackathon will rely on the use of COMPASS (COMputing Platform of Adaptive opticS System), an end-to-end simulation tool for AO system, allowing the users to generate synthetic but realistic AO loop data as if they were operating an actual AO system.

Level: intermediate

Reason for attending

- Actively contribute to current R&D for the largest astronomical telescopes, aiming to evidence new exoplanets and habitable worlds
- Learn more on applying AI / DNNs to real world use cases
- Have fun with advanced technologies for simulating complex cyber-physical systems

Presenter



Damien holds a PhD in Observational Astronomy from Université Paris-Diderot (2005). He has been an Adaptive Optics (AO) fellow, responsible for the last stages of commissioning of the Altair AO system on the Gemini North Telescope in Hawaii (2006) ; and an Instrument Scientist (2007-2008), for GeMS, the Gemini MCAO System, a facility featuring 6 Laser guide stars.

Since 2008, at Observatoire de Paris - PSL, Damien has been leading an original research program on high performance numerical techniques for astronomy including modeling, signal processing and instrumentation for large telescopes. He has been the P.I. of several large programs at national and European levels targeting AO Real-Time Controllers for giant optical telescopes with emerging computing technologies. Since 2021, with France officially joining SKAO, he is also getting strongly involved in the French effort dedicated to the construction of this giant radio-telescope. In particular, he is currently the inaugural head of ECLAT, a joint laboratory between CNRS, INRIA and Atos/Eviden, as a long-term support structure federating resources from academic and industrial teams that will engage in the R&D work for the French contribution to the SKA.

Tutorials and hackathon are scheduled 9:00 – 10:30 and 11:00 – 12:30 in the morning, and 14:00 – 15:30 and 16:00 – 17:30 in the afternoon.



Ada-related activities and the future evolution of the Ada programming language

During the banquet, attendees will have the opportunity to know more about the ongoing initiatives to strengthen the Ada community

SOCIAL EVENTS

The program includes coffee breaks and lunches at the conference location, providing the opportunity for participants to discuss their work, and to socialise. Other social and networking events are planned for the conference week

Tuesday, June 11th

The first social event is a **Welcome Visit and Dinner**, which will take place on **Tuesday, starting at 17:45** and will feature two moments. First, **from 17:45 until 19:15** we will stay at the picturesque gardens of Torre Girona, in front of the chapel. During this first part, participants will enjoy a taste of local wines paired with the renowned Iberian ham while they also have the unique opportunity to explore the Marenostrum V. Inaugurated in December 2023, this supercomputer is on track to reach its maximum capacity of 311 .95PFLOPS.



Then, **from 19:30** participants will be able to enjoy an excellent cocktail dinner (partly sponsored) in the Jardí de l'Abadessa restaurant, at 15 minutes walk from the first part of the reception. With its lush greenery and serene atmosphere, the restaurant provides an ideal setting for attendees to unwind and engage in meaningful conversations prior to the commencement of the main conference sessions.



Wednesday, June 12th

The **conference banquet** is scheduled for **Wednesday, June 12, from 20:00 to 23:00**, at the emblematic restaurant "7 portes".

Attendees will have the opportunity to savor the finest flavors of the Catalan and Mediterranean cuisines. Among the culinary delights awaiting you is the renowned "Paella Perallada", a masterpiece that harmoniously combines semi-dry rice with succulent peeled shellfish, delectable seafood and tender meats.



With a history spanning over 180 years, "7 portes" stands as a witness to the evolution of some of the most illustrious artists of their time, including Pablo Picasso and Antoni Tàpies. Their presence has left an indelible mark, forming a captivating small art gallery within the restaurant's walls, waiting to be discovered by guests. The space is situated within the historic "Casa Xifré", one of Barcelona's most iconic landmarks, in the charming neighborhood of Sant Pere-Santa Caterina i la Ribera and nestled mere meters away from the bustling Port of Barcelona and the "Llotja de Barcelona" (the fish market).



Thursday, June 13th

The organization has carefully prepared a (optional) chill out event as a culmination for this year's main conference. The event is scheduled for **Thursday, June 13, from 19:15 to 23:15**, at the Moritz Barcelona Brewery, the brewery of the first beer of Barcelona. This event is partly sponsored, and divided in three parts:

First, a visit to the Moritz Brewery, promising an immersive experience. Lasting approximately 45 minutes, attendees will delve into the intricate secrets of beer production, gaining insight into one of the world's most modern microbreweries.

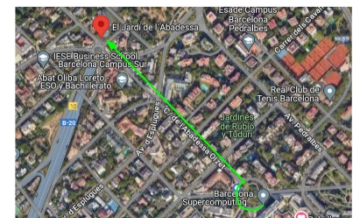
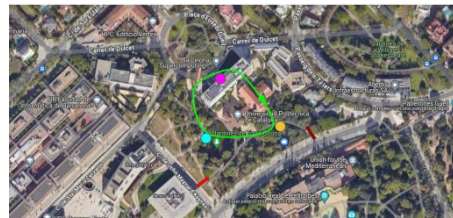
Then, attendees will be greeted with a warm welcome drink at the Brasserie room, on the -1 floor of the Moritz Factory, offering an exclusive vantage point overlooking the maceration tanks. Here, attendees can unwind and reconnect with fellow AEiC community members, indulging in a curated selection of Moritz beers, fine Catalan wines, and refreshing beverages.

The culinary journey continues with a banquet served within the same Brasserie room. Renowned chef Jordi Vilà, adorned with a Michelin star, has meticulously crafted a menu that harmoniously blends the finest local flavors with Moritz beers and Catalan wines.



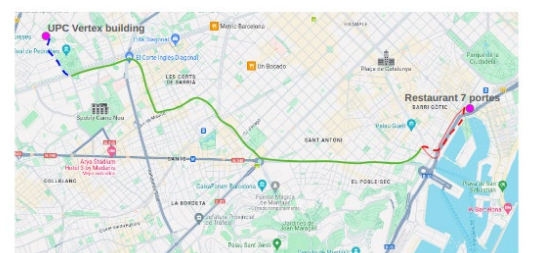
TRANSPORTATION IN BARCELONA

Tuesday events are on a walking distance from the conference venue. Refer to the maps on the right and the information on the conference website for the access to the visit and the path between BSC and the restaurant.



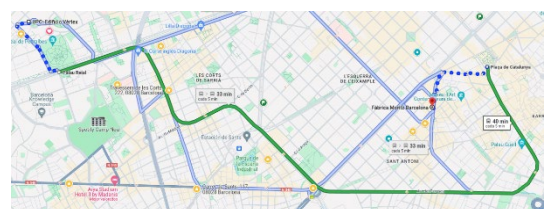
- Plaça d'Eusebi Güell, 1-3, 08034, Barcelona
- Carrer de John Maynard Keynes, 30, 08034, Barcelona
- Carrer de Jordi Girona, 08034, Barcelona
- Welcome reception (Part 1)
- Barcelona Supercomputing Center, Marenostrum V
- Torre Girona lake

Wednesday and Thursday events are located in the city centre. On Wednesday, it will take about 45 minutes to get to the restaurant from UPC building. Our recommendation is to take the L3 metro at "Palau Reial" station, direction "Trinitat Nova" and get down in "Drassanes" station. Afterwards, we highly recommend taking a leisurely 15-minute stroll along the picturesque Port of Barcelona. Alternatively, walk 3 min to "La Rambla" and catch the V13 bus at the "La Rambla - Santa Mònica" station, heading towards "Pla de Palau". Alight at "Pla de Palau - Metro Barceloneta". From there, a 2-minute walk will lead you directly to the restaurant.



- Walk from UPC Vertex building to "Palau Reial" L3 (green line) metro station
- Take the metro direction "Trinitat Nova" and stop at "Drassanes" station
- Walk to "Restaurant 7 portes"
- Alternatively, take the V13 bus at "La Rambla - Santa Mònica" direction "Pla de Palau" 4 stops until "Pla de Palau"

On Thursday, for those attending the chill-out event, recommend to take the L3 metro at "Palau Reial" station, in the direction of "Trinitat Nova" until the "Plaça Catalunya" station. From there, it's a 12-minute walk to reach the brewery.



Attendees can find more directions and maps on the conference website.

CORE CONFERENCE COMPOSITION

The core conference program features four distinct types of technical presentations, plus a panel session, all with different duration, all followed by various manners of discussion time. In the visual synopsis of the program schedule shown ahead, each distinct presentation type is denoted by a specific colour code.

Technical Contribution Type	Colour Code	Duration (including Q&A)
Keynote talk		1 hour
Panel		1 hour
Invited Talk		30 minutes
Journal-track talk		25 minutes
Industrial-track talk		15 minutes
Work-in-progress-track talk		10 minutes
Vendor presentation		15 minutes

It is a characterizing trait of the AEiC conference series that the presentations of such diverse contributions are combined into by-theme and not by-track presentation sessions, in order that authors and participants alike all enjoy all flavours of the program in a mixed as opposed to segregated combination. All works presented have undergone peer review, with track chairs assuring that the process was free of conflict of interests between authors and reviewers.

CORE CONFERENCE SCHEDULE

	Wednesday, 12 th June	Thursday, 13 th June
9:00 – 9:15	Welcome and opening (conference chair)	
9:15 – 10:15	Keynote Talk Chair: Björn Andersson <i>Strategies to build safety relevant high-performance HW/SW platforms for critical embedded systems</i> Francisco J. Cazorla, Jaume Abella, BSC, Spain	Panel Chair/Moderator: Cristina Secleanu <i>AI for Safety-Critical Systems: How "I" Should the AI be?</i> Kerstin Bach , Norwegian University of Science and Technology, Irene Yarza , Ikerlan, Marta Barroso , BSC
10:15 – 11:00	Refreshment break	Refreshment break
11:00 – 12:30	Session 1: Fault Tolerance and Reliability in Heterogeneous Systems Chair: Tullio Vardanega <i>HyFAR: a cost-effective Hypervisor-based Fault tolerance Approach for Heterogeneous Automotive Real-time Systems</i> J. Lex, R. Mader, M. Ulrich, D. Fey	Session 4: Machine Learning and Optimization for Embedded Systems Chair: Kerstin Bach <i>MLino Bench: A Comprehensive Benchmarking Tool for Evaluating ML Models on Edge Devices</i> V.-E. Baciú, J. Stiens, B. Da Silva
	<i>Enhancing Scalability of Static Code Analysis through Graph Database and Pattern Matching</i> Q. Dauprat, P. Dorbec, G. Richard, J.-P. Rosen	<i>An Autoencoder Architecture for Network Intrusion Detection in Embedded Systems</i> N. Borgioli, F. Aromolo, L. T. Xuan Phan, G. Buttazzo
	<i>EUROCITY Presentation</i> Emma Claus	<i>Gradient Descent Algorithm for the Optimization of Fixed Priorities in Real-Time Systems</i> J. M. Rivas, J. J. Gutiérrez, A. Guasque, P. Balbastre
	<i>FDN (Flexible Digital Network) for RTOS in the Automotive Industry</i> R. Llorca, I. Alconada, A. Montiel	<i>Software verification and Generative AI – Some practical examples and considerations</i> M. Martignano, A. Damiani, D. Gui, S. Magalini, L. Nucciarelli
	<i>Re-configurable and Scalable Honeynet for Cyber-Physical Systems</i> L. Sousa, J. Cecílio, P. Ferreira, A. Oliveira	
12:30 – 13:30	Lunch	Lunch

	Wednesday, 12 th June	Thursday, 13 th June
13:30 - 14:00	Invited Talk Chair: Sara Royuela <i>Simplifying the life-cycle management of complex application workflows</i> Rosa Maria Badia , BSC, Spain	Session 5: Real-Time Systems and Their Analysis Chair: Alejandro Mosteo <i>Toward Linux-based safety-critical systems – Execution time variability analysis of Linux system calls</i> M. Galarraga , C.-A. Lefebvre, J. Perez-Cerrolaza, J. A. Pascual
	Session 2: Software Verification and Code Generation Chair: Hai Nam Tran <i>Modelling Task Priority in Symbolic Predictive Analysis for Embedded Software in Ada</i> R. Krishnan, A. Gupta	<i>Using MAST for Modeling and Response-Time Analysis of Real-Time Applications with GPUs</i> I. Gomez , U. Díaz de Cerio, J. Parra, J. M. Rivas, J. J. Gutiérrez, M. González Harbour
14:00 - 15:00	<i>A Framework for Static Analysis and Verification of Low-Level RTOS Code</i> V. Manjunath , M. Baunach	<i>Using AdaCore's GNAT for CUDA for Safety Critical GPU Code Development and Verification</i> D. Aspetakis, M. M. Trompouki , L. Kosmidis, J. Ruiz, G. Marosy
	<i>Algebraic Effects and Static Analysis for Safety-Critical Applications in Fuzion</i> F. Siebert , M. Lill, M. Teufel	<i>An Iterative Benchmark Configuration Method for Quantifying Multi-Core Interference</i> S. Levieux, F. Singhoff , S. Rubini, P. Plasson, P.-V. Gouel, L.-R. Malac-Allain, L. Miné, G. Brusq
	<i>Task-to-Thread Mapping in OpenMP Using Fuzzy Decision Making</i> M. Samadi , T. Carvalho, L. M. Pinho, S. Royuela	
15:00 - 15:30	Invited Talk Chair: Luis Miguel Pinho <i>The Compute Continuum: An Efficient Use of Edge-to-Cloud Computing Resources</i> Eduardo Quifones , BSC, Spain	Refreshment break
15:30 - 16:00	Refreshment break	Session 6: Advancements in RTOS and Embedded Software Development Chair: Irune Yarza <i>Unishyper: A Rust-based Unikernel Enhancing Reliability and Efficiency of Embedded Systems</i> B. Jiang , K. Hu, W. Huang, L. Wang, C. Mo, Y. Chen, J. Ren
16:00 - 17:30	Session 3: Safety and Security in Embedded Systems Chair: Matthias Becker <i>Zero-Trust Design and Assurance Patterns for Cyber-Physical Systems</i> S. Hasan , I. Amundson, D. Hardin	<i>The MATERIAL Framework: Modeling and AuTomatic Code Generation of Edge Real-Time Applications under the QNX RTOS</i> M. Becker , D. Casini
	<i>Assuring the Safety of Rechargeable Energy Storage Systems in Electric Vehicles</i> F. Ul Muram , M. Atif Javed, P. Pop	<i>HiRTOS: A Multi-Core RTOS written in SPARK Ada</i> J. G. Rivera <i>Supporting Ada in the ROSE compiler</i> P. Pirkelbauer , C. Liao, P.-H. Lin, D. Wright, C. Reynolds, D. Quinlan
	<i>Implementing Unsafe Features on top of a Safe Intermediate Language</i> S. T. Taft	<i>Improving availability in a robotic application without loss of safety</i> G. Rincon , C.-F. Nicolas, T. Poggi
17:00 - 17:30	<i>Software-based Security Framework for Edge and Mobile IoT</i> J. Cecilio , A. Sá, A. Souto	Awards & Future events Closing of Core Program
	<i>A Framework for Improving Portability and Ensuring Correctness of Operating System Kernels</i> V. Manjunath , M. Baunach	

CO-LOCATED EVENTS: FRIDAY, JUNE 14TH

9th International Workshop: *Challenges and new Approaches for Dependable and Cyber-Physical Systems Engineering (DeCPS 2024)*

<http://www.ada-europe.org/conference2024/decps.html>

Organizers

- Alessandra Bagnato, SOFTEAM, France
- Barbara Gallina, Mälardalen University (MDU), Sweden
- Daniela Cancila, CEA LIST, France
- Laurent Rioux, Thales, France
- Luis Miguel Pinho, ISEP, Portugal

Synopsis

In recent years, the Internet of Things (IoT) has experienced an extraordinary development with large impact on society; however, there is still a gap between the physical and the cyber worlds. Cyber Physical Systems (CPS) constitute a new class of engineering systems, which integrate software control and autonomous decision making with signals from an uncertain and dynamic environment. In the context of cyber systems, Artificial Intelligence (AI) technologies can contribute to manage a huge amount of heterogeneous data that come from different sources without human intervention. CPS technology transformed the way people interact with engineering systems, in a very wide spectrum of applications: smart mobility, autonomous driving, digital healthcare, smart grids and buildings, mobile co-operating autonomous robotic systems, digital consumer products and services, etc.

The DeCPS workshop is a collaboration event, providing a platform to industrial practitioners, researchers, and engineers in academia to exchange of their ideas, research results, experiences in the field of dependable and cyber physical systems engineering, from a theoretical as well as a practical perspective. Following the workshop tradition, the 2024 edition will consist of presentations of applied research in the area, as well as a discussion session on future challenges and potential collaborations.

Proceedings

The DeCPS organizers will produce post-event proceedings, with all presented papers and summary of the discussions, to appear in due course in the Ada User Journal.

Program

Friday, 14 th June	
09:15 - 9:30	Welcome and opening (Luis Miguel Pinho)
	Session 1
09:30 - 10:30	<i>AI Augmented Requirements Engineering in the AIDOaRT project: NLP Techniques and Language Models to Encode Requirements Text Semantically for the Railway Industry</i> Alessandra Bagnato, Bilal Said
	<i>5G-enabled edge computing for real-time smart mobility applications: The PROXIMITY platform</i> Elli Kartsakli
10:30 - 11:00	Refreshment break

	Session 2
11:00 - 12:30	<i>Towards Model-based System Engineering for Cyber Physical Systems in the MYRTUS project</i> Alessandra Bagnato , Juan José Cadavid
	<i>Improving and leveraging OpenMP for the efficient and safe use of new high-performance hardware platforms: The LIONESS project</i> Sara Royuela
	<i>Design Space Exploration using Evolutionary Optimisation in Cyber-Physical Systems: A Smart Port Case Study</i> Ken Sharman, Sergio Sáez , Javier Coronel
12:30 - 14:00	Lunch
14:00 - 15:00	Discussion: future challenges and potential collaborations
15:00 - 15:15	Workshop closing

3rd International Workshop: *AADL by its practitioners (ADEPT)*

<https://adept.univ-brest.fr/2024/>

Organizers

- Jérôme Hugues, Software Engineering Institute, Carnegie Mellon University, USA
- Frank Singhoff, Lab-STICC/Univ. of Brest, France
- Hai Nam Tran, Lab-STICC/Univ. of Brest, France

Event sponsor



Synopsis

The Architecture Analysis and Design Language (AADL) is an SAE International Standard dedicated to the precise modeling of complex embedded systems, covering both hardware and software concerns. Its definition relies on a precise set of concepts inherited from industry and academic best practices: clear separation of concerns among layers, rich set of properties to document system metrics, and support for many kinds of analysis: scheduling, safety and reliability, performance, and also code generation.

The AADL standard is now a mature standard for the modeling of critical embedded real-time systems. AADL defines a language and supporting tools for the precise modeling and analysis of systems. AADL is today employed by numerous stakeholders in the domain of critical embedded real-time systems to address a large set of concerns: performance (latency, schedulability), safety, or security. One key strength of AADL as a language is the set of tools that provide analysis capabilities.

The ADEPT workshop aims to present and report on current projects in the field of design, implementation, and verification of critical systems where AADL is a first-citizen technology. The ADEPT workshop is also an opportunity for AADL beginners to meet experienced AADL practitioners.

ADEPT24 would be the third workshop edition. It is a full-day workshop. The workshop is dedicated to the presentation of research around ADDL, AADL new technologies, and success stories. A return of experience in the form of a discussion with the attendees will close the workshop. It is open to anyone interested in AADL and in the design and verification of software architecture for critical systems.

Proceedings

A post-workshop proceeding will be published in the Ada User Journal that summarizes the workshop talks and also the workshop discussions co-authored by all participants.

Program

Time	Session	Presentation
09:00 - 09:30	Workshop opening	Introduction and news about AADL <i>Bruce Lewis</i>
09:30 - 10:30	Session 1: UAV	UAV autopilot architectures versus AADL <i>Emmanuel Grolleau</i>
		Safe UAV Continuous-Control Architecture Design <i>Leandro Buss Becker, Fernando Silvano Gonçalves, Elton Ferreira Broering, Henrique Amaral Misson and Lucas Cordeiro</i>
10:30 - 11:00		Coffee break
11:00 - 12:30	Session 2: Model-based System Engineering	TASTE and AADL in the METASAT Model-Based Engineering Workflow <i>Alejandro Calderón, Irune Yarza, Stefano Sinisi, Lorenzo Lazzara, Valerio Di Valerio, Giulia Stazi, Leonidas Kosmidis, Matina Trompouki, Alessandro Ulisse, Aitor Amonarriz and Peio Onaindia</i>
		AQDT-GEN: AADL and QEMU-based Digital Twin generation for IoT testing <i>Monica Michelle Villegas Arias, Hernan Astudillo and Faber Giraldo</i>
		Executable AADL Models for Early System Qualification Test <i>Stéphane Rubini, Sébastien Leveux, Eric Cariou, Frank Singhoff, Hai Nam Tran and Gilles Le Pluart</i>
12:30 - 14:00		Lunch break
14:00 - 15:30	Session 3: AADL tools update	INDIGO - Collaborative MBE across Diverse System Models Including AADL <i>Steve Vestal and Ed Sandberg</i>
		CAMET: Curated Access to Model-based Engineering Tools <i>Bruce Lewis</i> <i>5-minute presentation</i>
		Ellidiss tools for AADL modeling and verification, and current state of the SysML v2 library for AADL support <i>Pierre Dissaux</i> <i>15-minute presentation</i>
		Multiprocessor schedulability analysis with AADL/Cheddar: how to handle various interference? <i>Frank Singhoff, Stéphane Rubini, Hai Nam Tran</i> <i>5-minute presentation</i>

Enabling the use of AI in Safety-Critical Systems (SafeAI)

Organizers

- Francisco J. Cazorla (Barcelona Supercomputing Center, Spain)
- Jaume Abella (Barcelona Supercomputing Center, Spain)

Synopsis

The increasing computing performance delivered by embedded platforms has made possible the realization of advanced and performance-hungry functionalities in real time. Those functionalities, often related to autonomous operation and/or to the comprehension of complex scenarios, largely rely on AI software as the only solution delivering sufficiently accurate results. However, both, AI software and powerful embedded computing platforms, are at odds with the development process of safety-critical systems, which is described by domain-specific standards and guidelines, such as ISO 26262 in automotive, DO178C and DO254 in avionics, and IEC 61508 for electronic industrial systems. Difficulties arise from (1) the need for "divide & conquer" strategies pursued by safety regulations, which aim at decomposing systems iteratively until having components sufficiently simple to be realized, understood and tested, and (2) the perceived black-box nature of AI software and high-performance computing devices, whose complexity cannot be broken down as needed by safety standards

Several public (e.g. EC funded projects) and private activities (e.g. AI-focused working groups) have started recently to address this challenge aiming at (1) making AI software explainable, with the term explainable often overloaded to refer to transparent, reliable, robust, and verifiable, among other desired characteristics of AI for safety-critical systems; (2) containing embedded platform complexity, especially when running AI software, using appropriate system software and middleware support; and (3) adapting safety regulations conceived for control software to admit the data-dependent and stochastic nature of AI software in the context of the development of (and use in) safety-critical systems.

This workshop will present a number of challenges in the form of industrial use cases building on AI, as well as the latest advances in terms of safety-relevant system development, AI solutions amenable for safety-critical systems, and system software and middleware support to contain and model platform complexity.

Program

Friday, 14 June 2024	
08:50 - 09:00	Welcome
Session 1 (09:00-10:30)	
09:00 - 09:05	Message by the Organizers <i>Jaume Abella / Francisco J Cazorla</i>
09:05 - 09:45	Deploying AI in space: benefits and challenges <i>Gabriele Giordanna (AIKO)</i>
09:45 - 10:30	Industrial Challenges for Mobile Robots <i>Francesco Ferro (PAL-ROBOTICS)</i>
10:30-11:00	Break

Session 2 (11:00-12:45)	
11:00-11:45	Functional Safety on AI-based critical systems <i>Irune Yarza (IKR)</i>
11:45-12:45	Panel on enabling the use of AI in critical systems <i>All Presenters</i>
12:45-14:00	Lunch
Session 3 (14:00-15:00)	
14:00-14:45	Integrating Probabilistic Uncertainty sources and Explainability in Critical AI Systems <i>Axel Brando (BSC)</i>
14:45-15:00	Wrap-up <i>Jaume Abella / Francisco J Cazorla</i>

Ada Developers Workshop

Organizers

- Fernando Oleo Blanco, Libre Ada Software Aficionado, irvise@irvise.xyz
- Fabien Chouteau, AdaCore, chouteau@adacore.com
- Dirk Craeynest, Ada-Belgium & KU Leuven, dirk.craeynest@cs.kuleuven.be

Synopsis

The Ada Developers Workshop aims to create an informal yet dynamic platform for developers in the Ada community to meet, share insights, and present their latest projects or project updates, using the Ada programming language and Ada-related technology such as SPARK. The topics will range from community advocacy all the way to technical presentations. The focus of the Developers Workshop will be in topics and projects that are widely used within the community and which help grow the Ada pool of users and the quality of life of existing programmers.

AEiC 2024 is an ideal fit for an Ada Developers Workshop. On the one hand, it gives the general community an opportunity to see what is happening in the Ada world and how Ada can help to produce reliable and efficient open software. On the other hand, it gives Ada projects an opportunity to showcase themselves, get feedback and ideas, and attract participants to their project and collaboration between projects.

Program

The full-day program is packed with 9 presentations on various Ada-related topics by 8 authors from 5 countries: Belgium, France, Italy, Spain, and USA. All time slots include Q&A. There will be extra time for participant interactions in between talks, and during breaks and lunch.

Friday, 14 th June	
09:00 - 9:05	Welcome (Fernando Oleo Blanco, Fabien Chouteau, Dirk Craeynest)
09:10-09:45	"SweetAda: a Multi-architecture Embedded Development Framework" Gabrielle Galeotti, Fernando Oleo Blanco

Friday, 14 th June	
09:50-10:25	<i>"Avoiding Access Types"</i> Jeffrey R. Carter
10:30-11:00	Refreshment break
11:00-11:30	<i>"G-NAV: Soaring the Clouds with AdaWebPack"</i> Guillermo A. Hazenbrouck
11:35-11:55	<i>"Alire 2.0: a Quality of Life Update"</i> Alejandro Mosteo
11:55-12:30	<i>"HiRTOS: a Multicore RTOS Written in SPARK Ada"</i> J. German Rivera
12:30-14:00	Lunch break
14:00-14:35	<i>"Ironclad: a Formally Verified OS Kernel Written in SPARK/Ada"</i> Cristian Simon
14:40-15:25	<i>"An Ada Story of Time"</i> Jean-Pierre Rosen
15:30-16:00	Coffee Break
16:00-16:25	<i>"Controlled I/O: a Library for Scope-Based Files"</i> Jeffrey R. Carter
16:30-17:25	<i>"Ada Community Advocacy"</i> Fernando Oleo Blanco
17:25-17:30	<i>"Closing Remarks"</i> Fernando Oleo Blanco, Fabien Chouteau, Dirk Craeynest

ORGANIZERS

Conference Chair

Sara Royuela
BSC, Spain

Journal track Co-Chairs

Björn Andersson
Software Engineering Institute -
Carnegie Mellon University, USA

Luis Miguel Pinho
ISEP & INESC TEC, Portugal

Industrial track Co-Chairs

Luciana Provenzano
Mälardalen University, Sweden

Michael Pressler
Robert Bosch GmbH, Germany

Work-in-Progress track

Co-Chairs

Alejandro R. Mosteo
CUD Zaragoza, Spain

Ruben Martins
Carnegie Mellon University, USA

Tutorial & Education Chair

Maria A. Serrano
NearbyComputing, Spain

Workshop Chair

Sergio Saez
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Spain

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White Elephant GmbH, Switzerland

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Dirk Craeynest
Ada-Belgium & KU Leuven, Belgium

Local Chair

Nuria Sirvent
BSC, Spain

Web Master

Hai Nam Tran
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